Abstract of the Disclosure

A packet processing device has an on-board match engine memory. Actions to be taken on a packet can be looked up in the match engine memory using a key comprising a match engine index and a protocol field from the packet. The match engine index is obtained from either a relatively small on-board parser memory or a larger context memory. The parser memory contains match engine indices for sparse protocols. Performance approaching that of hard-wired packet processors can be obtained. New protocols or changes in protocols can be accommodated by writing new values into the match engine, parser and context memories. The packet processing device can be provided in a pipelined architecture.